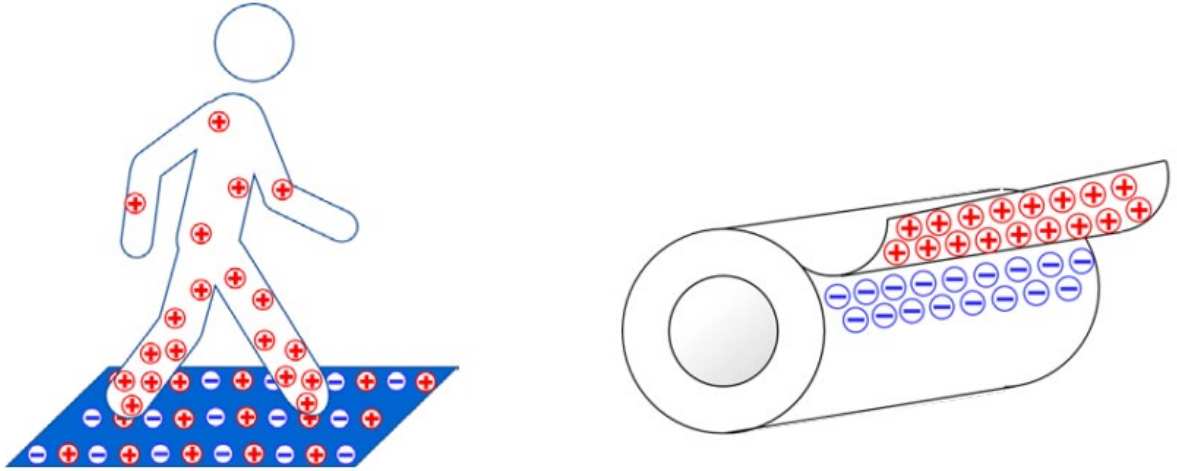
Live Lecture Series #2

Designing ESD Safe Circuits

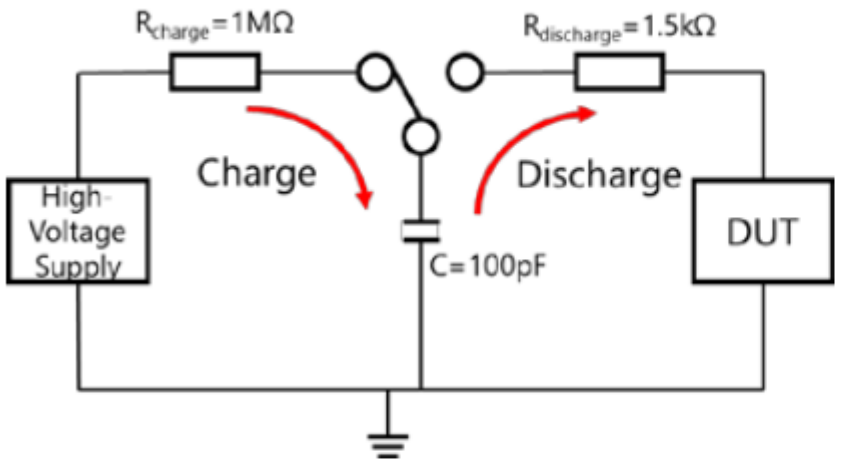
What Exactly Is ESD?

- **ElectroStatic Discharge (ESD):** is the release of static electricity when two objects come into contact.
- **Device level ESD:** An event that occurs to an unmounted semiconductor in an ESD controlled environment.
- **System level ESD:** An event that occurs to a finished electronic device/widget.

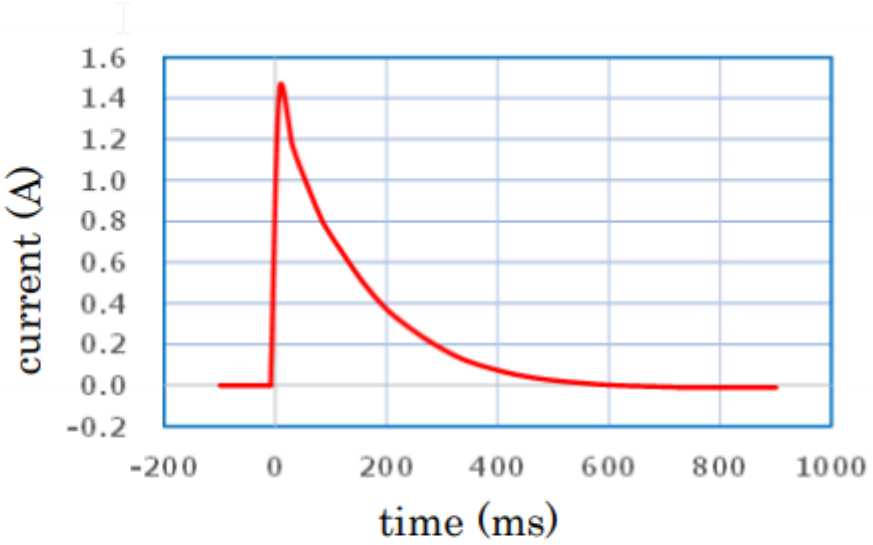


Basics of ESD Protection (TVS) Diodes - Toshiba

Device Level Tests



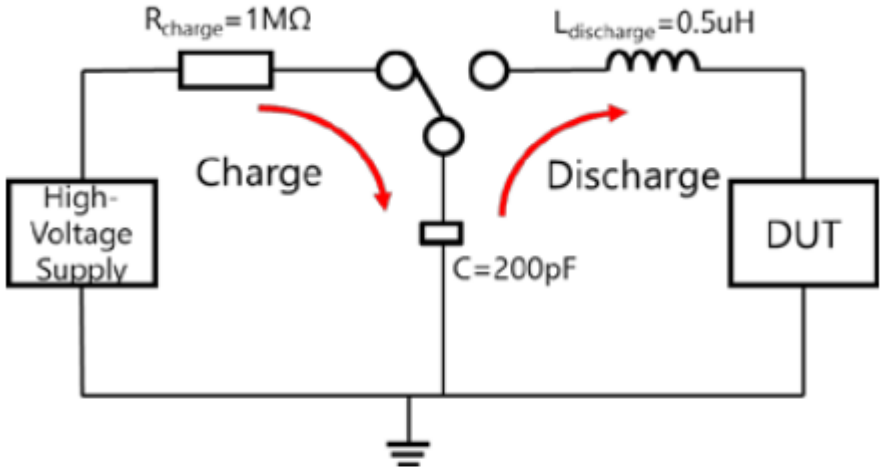
Test circuit example



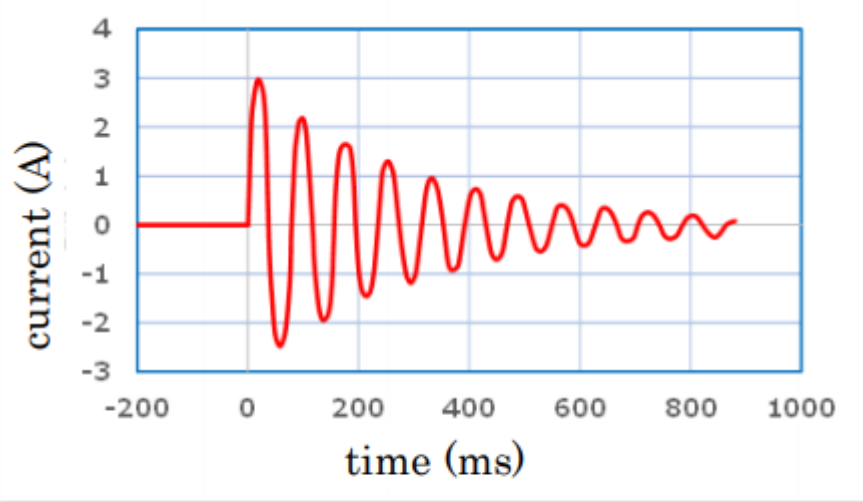
Test waveform example

Human body model (HBM)

Device Level Tests (cont'd)



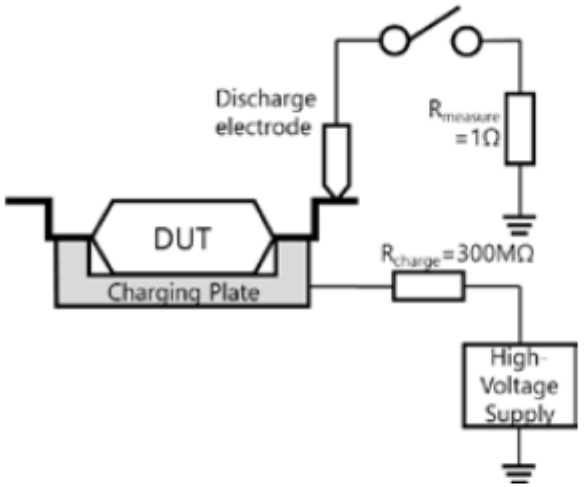
Test circuit example



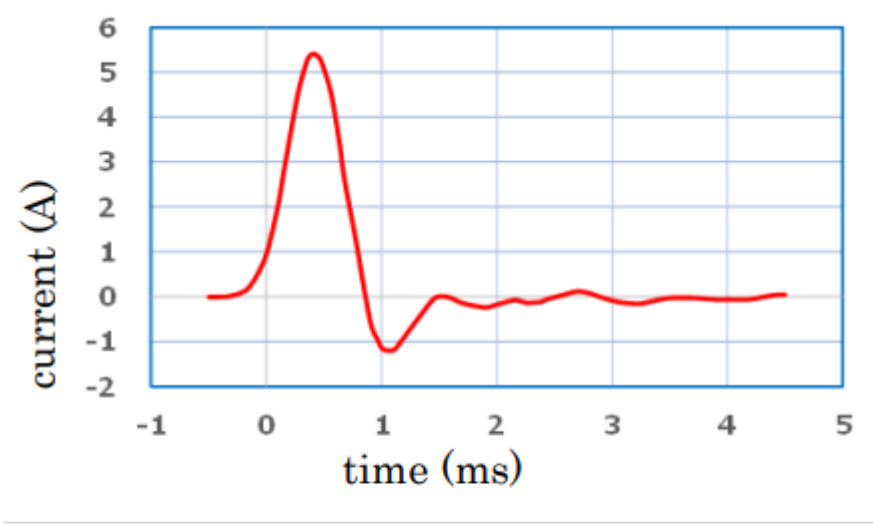
Test waveform example

Machine model (MM)

Device Level Tests (cont'd)



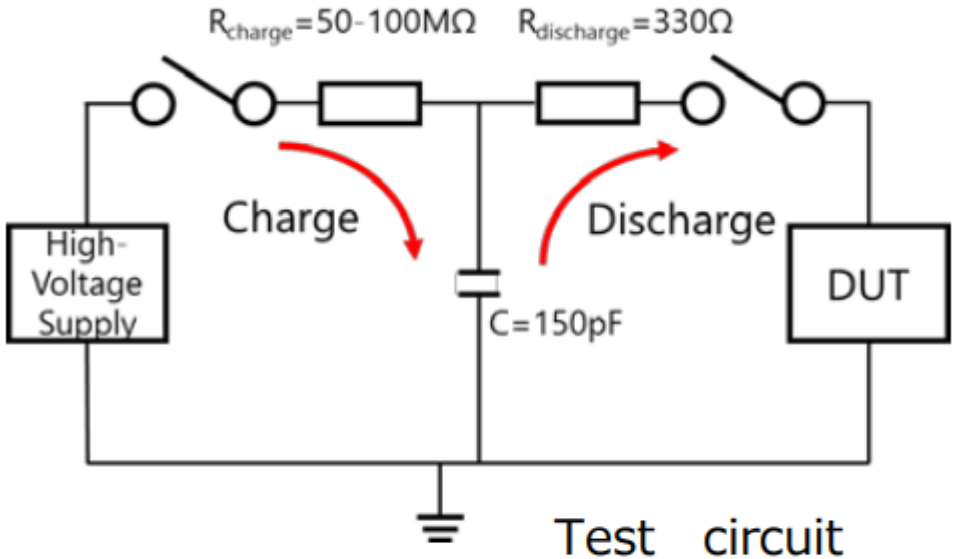
Test circuit example



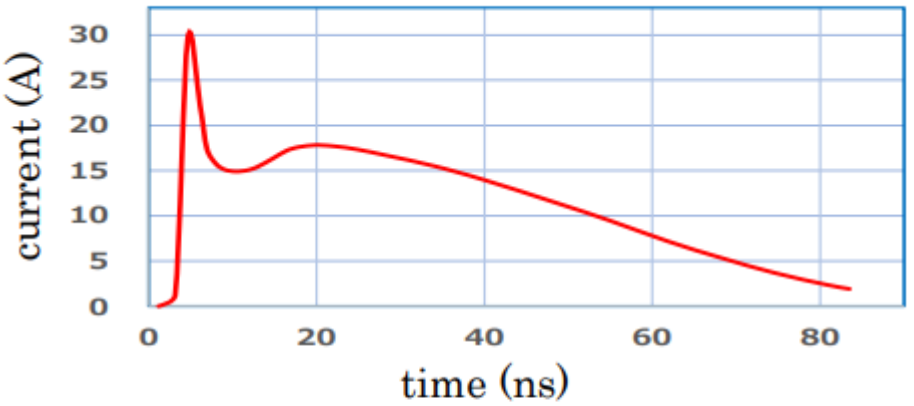
Test waveform example

Charged-device model (CDM)

System Level Tests



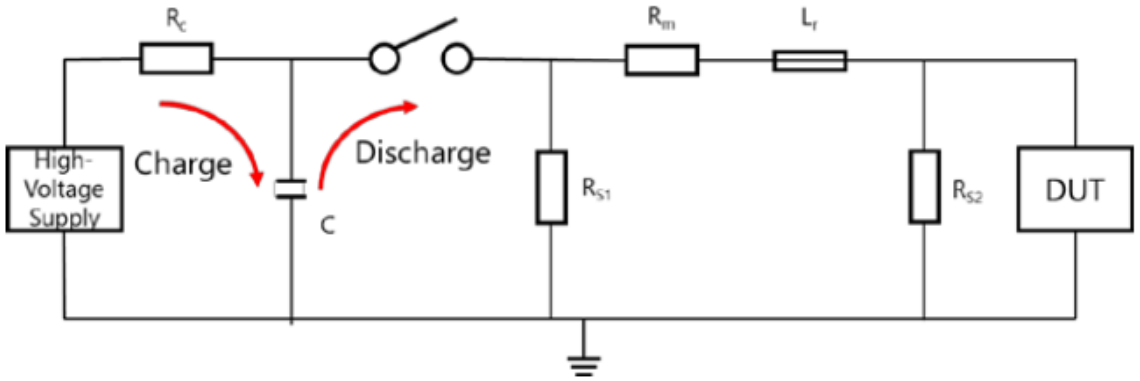
Test circuit



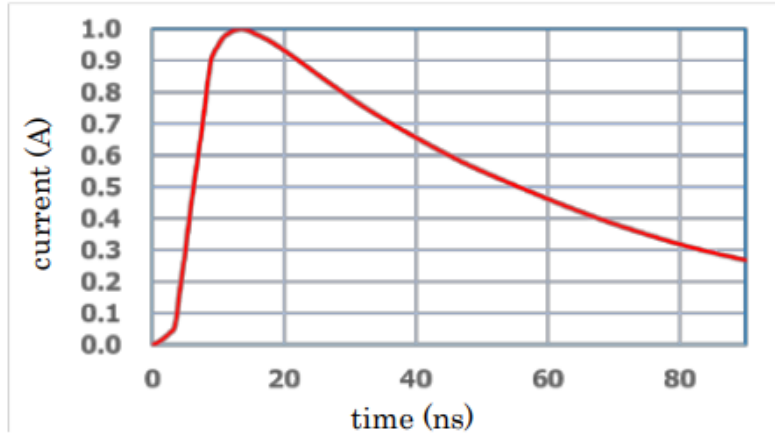
Test waveform example

IEC 61000-4-2 test

System Level Tests (cont'd)



Test circuit example



Test waveform example

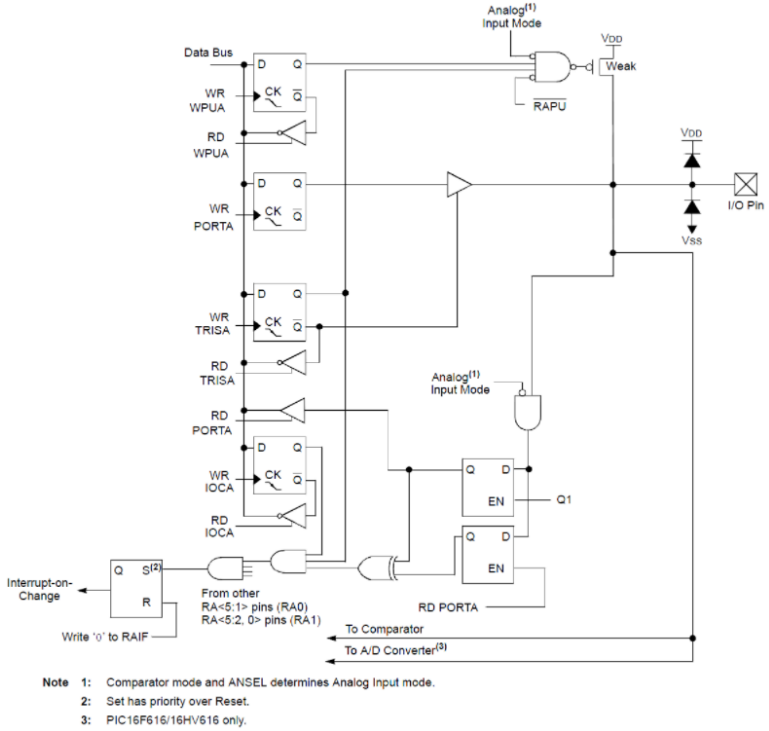
IEC 61000-4-5 test

What Is the Result of a System Level ESD Event?

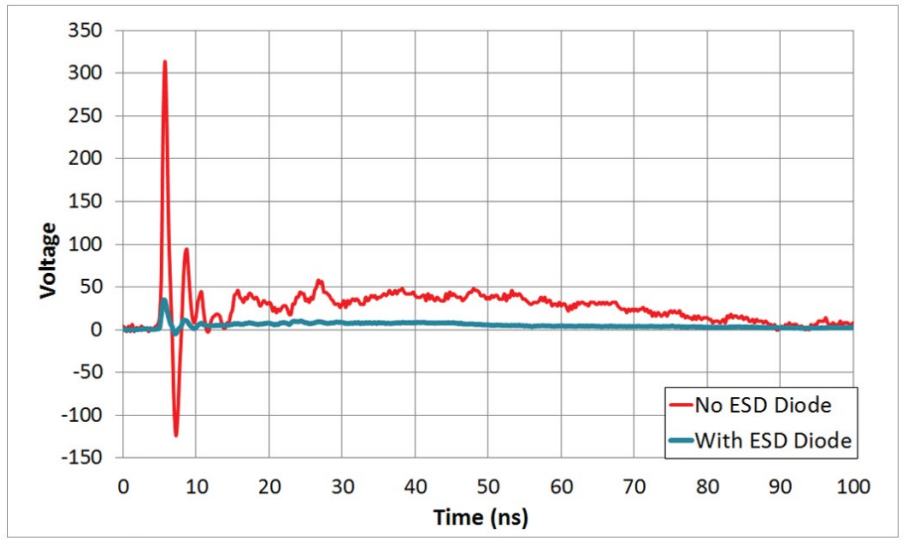
- No damage at all, system continues as normal
- **Soft Failure:** No physical damage, but the system has a “lockup” or “freeze.” May require physical intervention (i.e., power cycle.)
- **Hard Failure:** Physical damage to the system, may or may not show it immediately (latent defect/failure are the worst).

What is Our Goal With Hardware ESD Protection?

- It is <u>not</u> to try and eliminate all events.
- We want to reduce the event both in voltage and current so the internal IC protection can handle it.

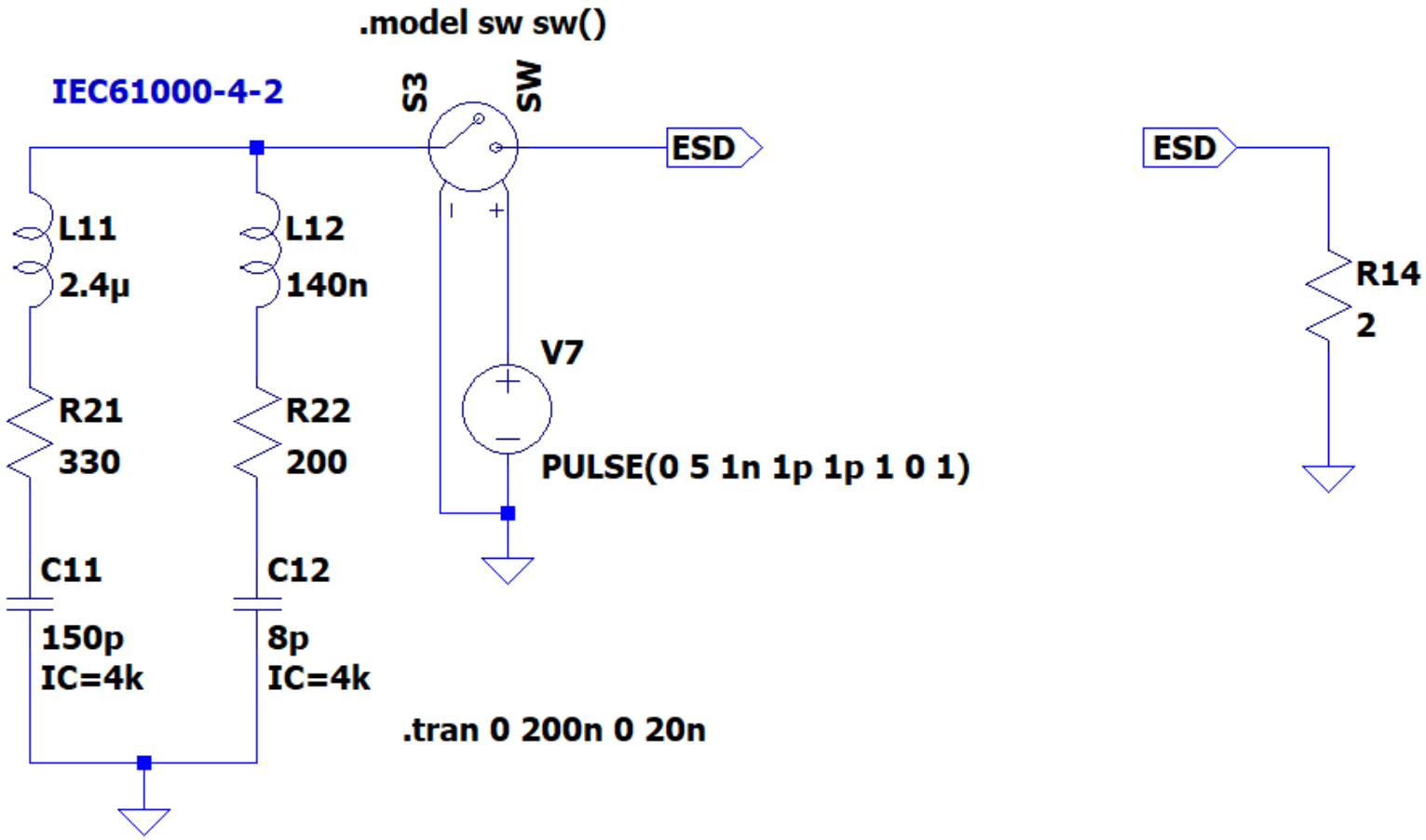


PIC16F616 - Microchip



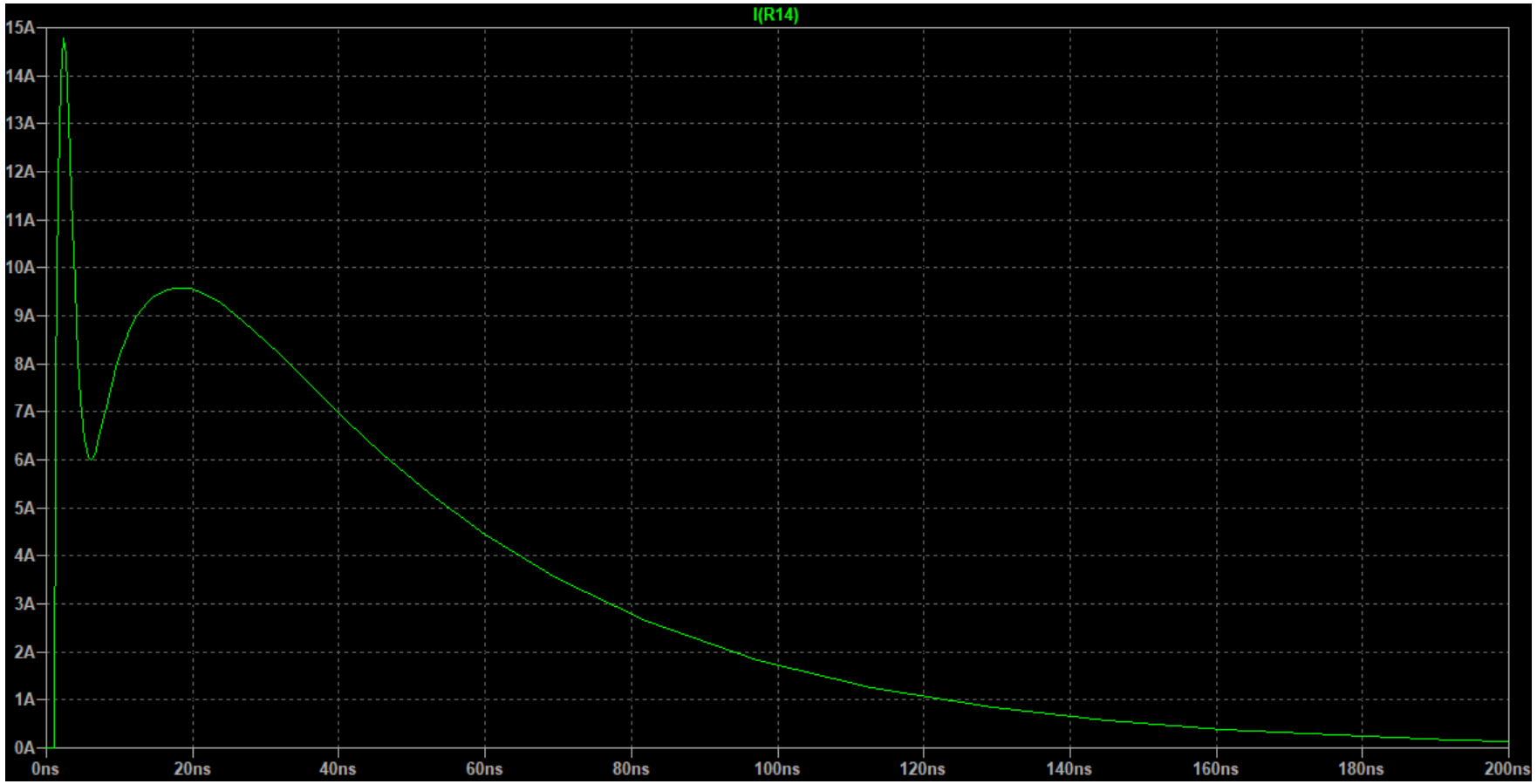
System-Level ESD Protection Guide – Texas Instruments

LTSpice Simulation IEC61000-4-2



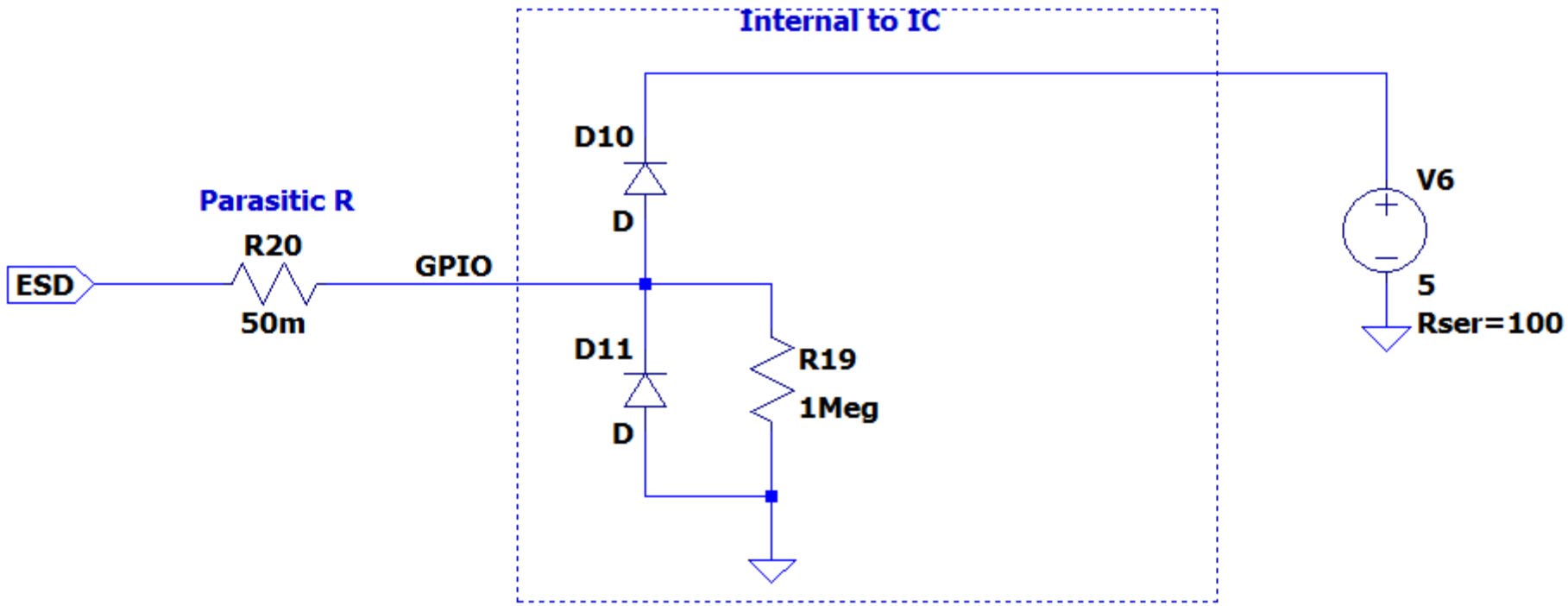
Based off: https://www.youspice.com/simple-spice-esd-generator-circuit-based-on-iec61000-4-2-standard/

LTSpice Simulation: Calibration

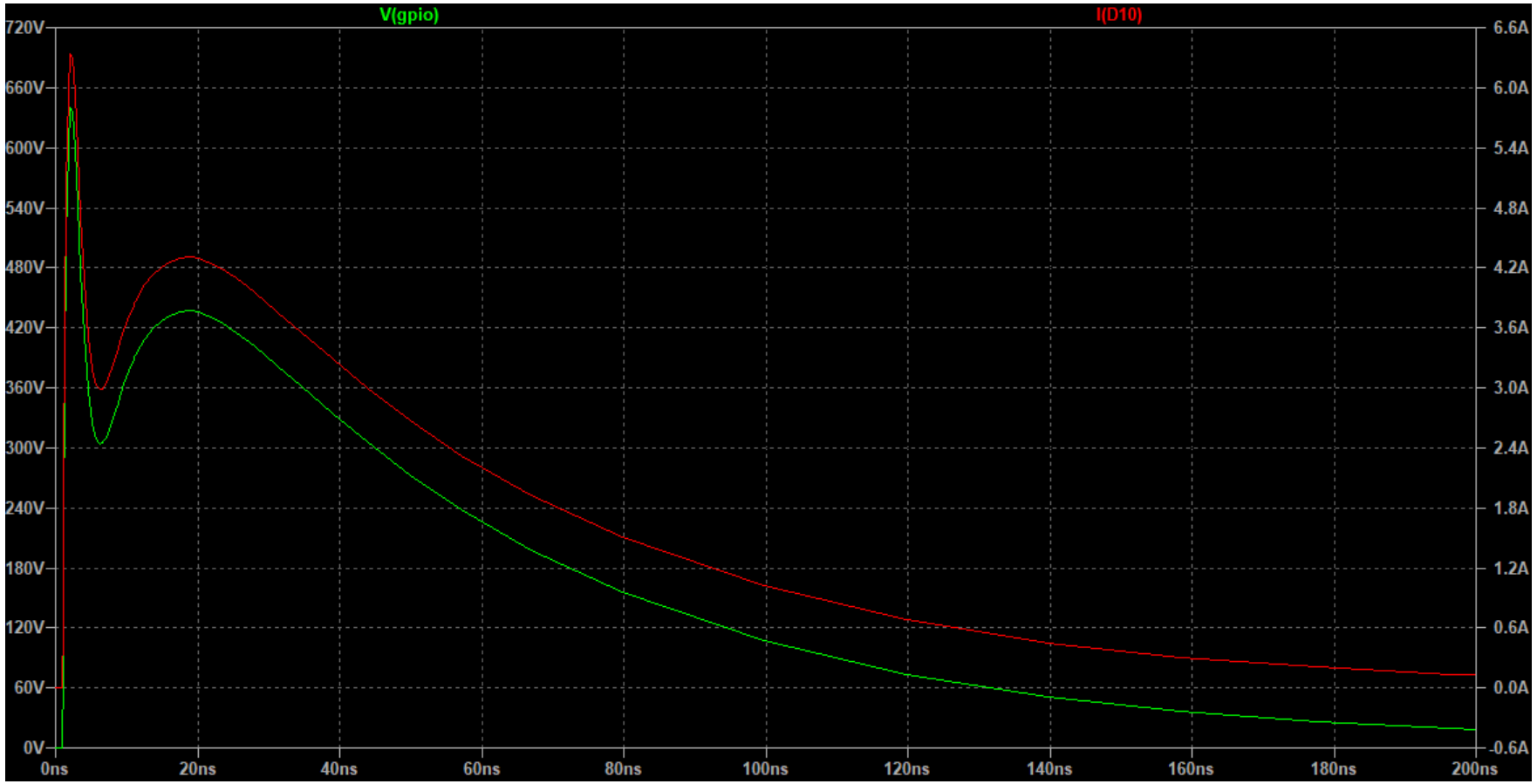


Using a 2R calibration resistor

LTSpice Simulation: No Protection

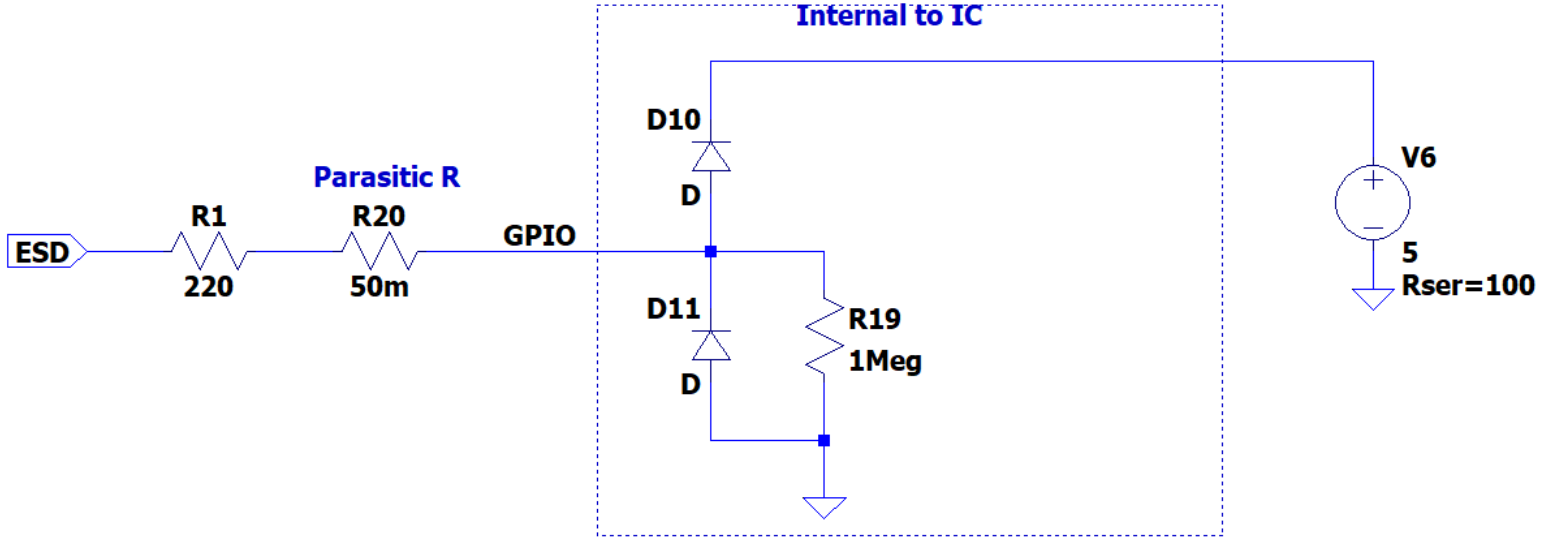


LTSpice Simulation: No Protection



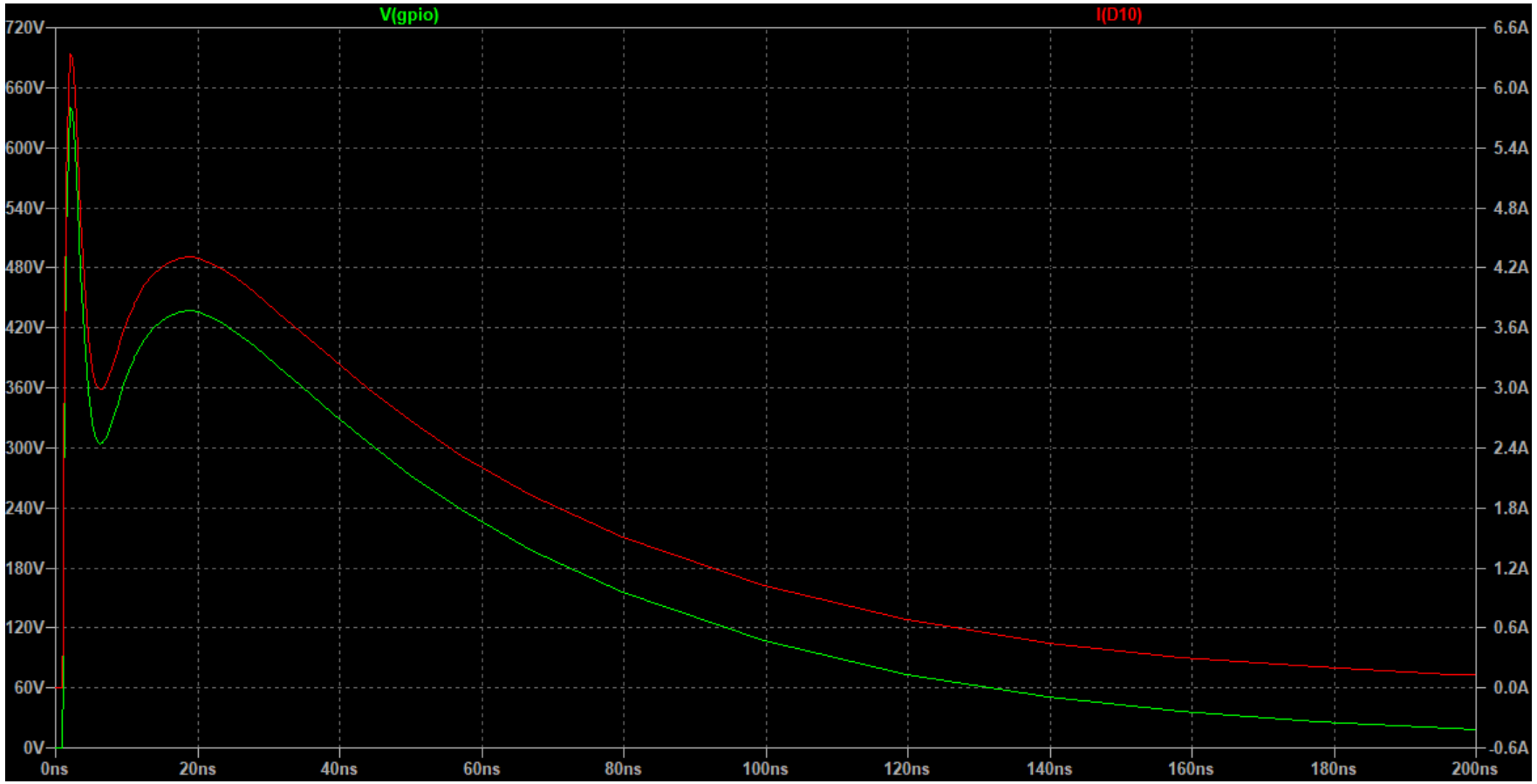
Strategy 1: Series Resistors

- Limits the peak current.
- Damp ringing.
- Help protect diodes downstream.
- Immensely helpful for general EMC and SI.



LTSpice Simulation: 220R Series Resistor

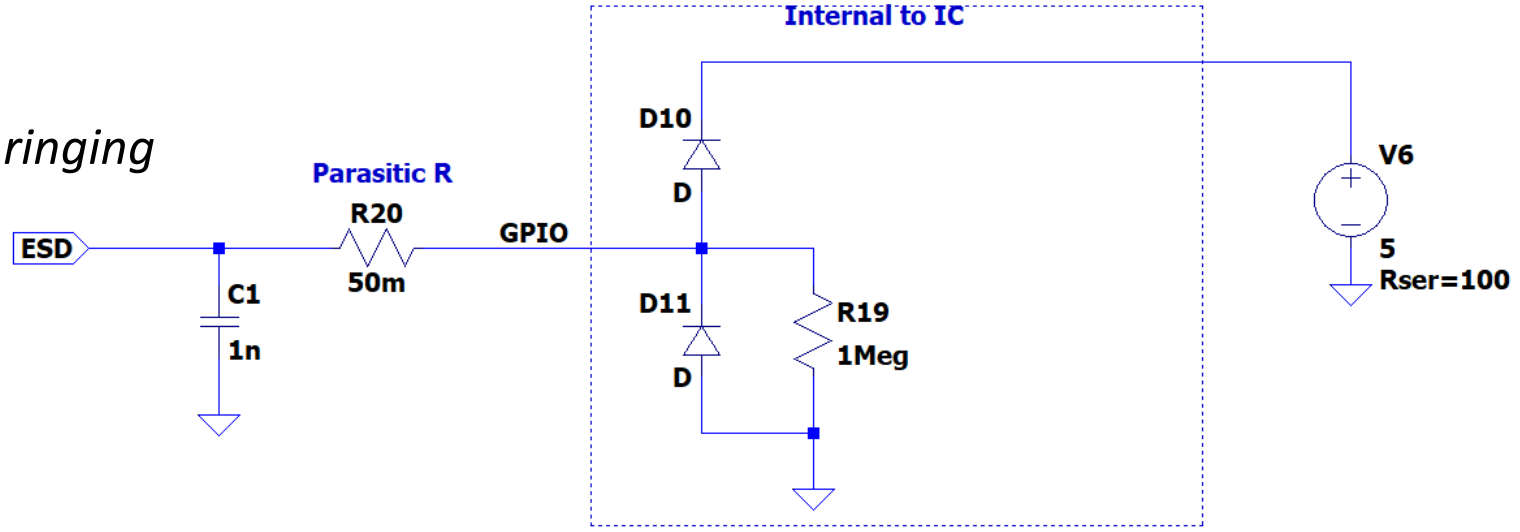
LTSpice Simulation: No Protection



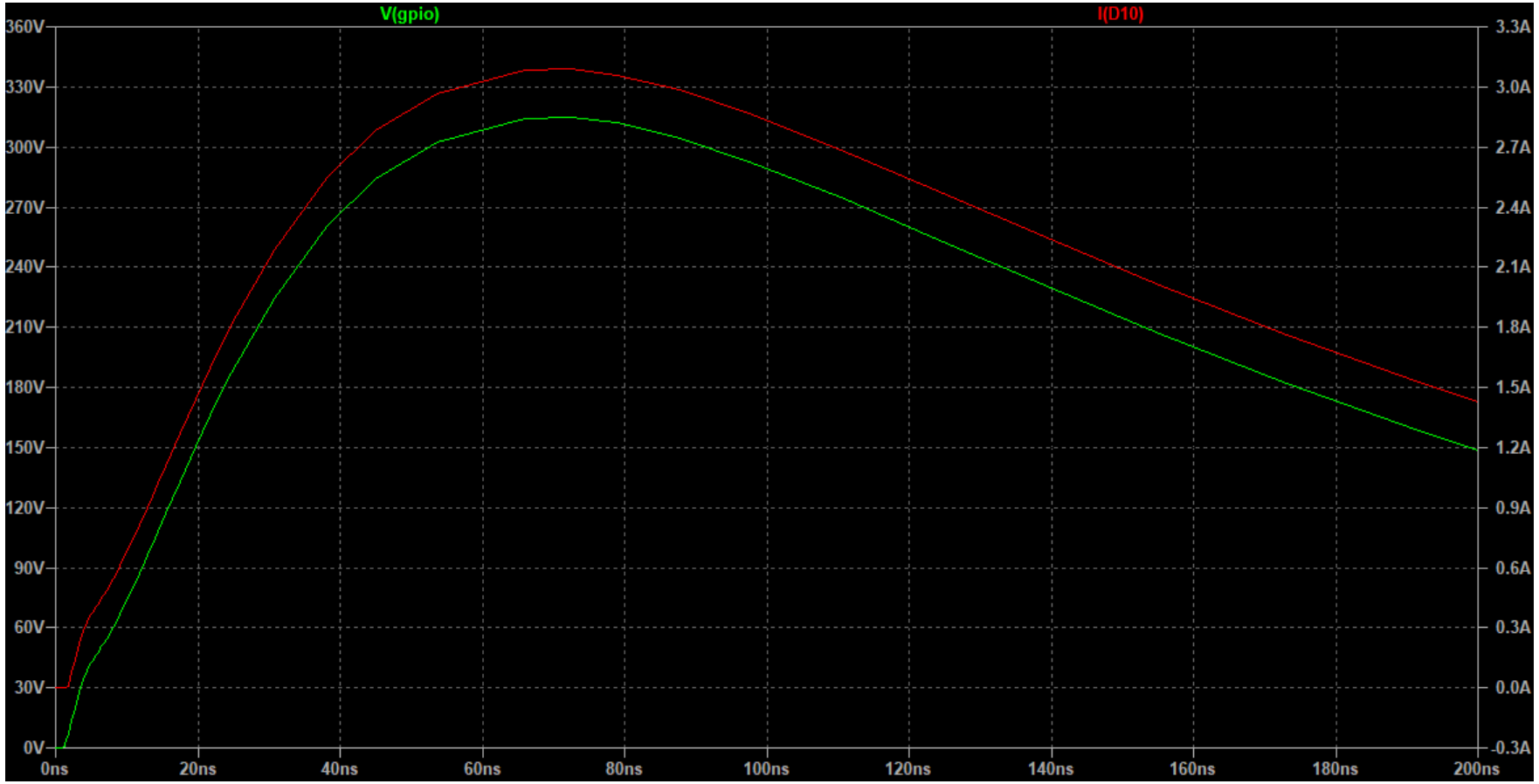
Strategy 2: Capacitors

- “Soaks up” the voltage spike.
- Smooths out the event.
- Higher the capacitor, the better it will perform*.
- Can’t use them on high-speed signals.

- **If not damped they can introduce ringing*



LTSpice Simulation: 1nF Ceramic Capacitor

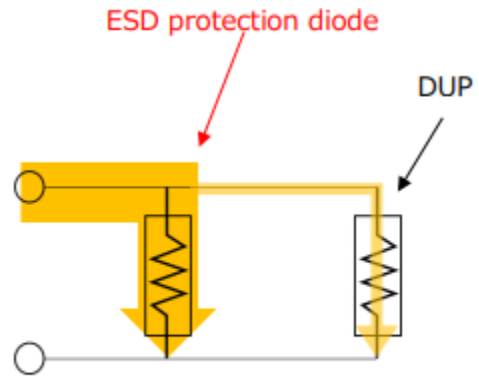


LTSpice Simulation: 220R Series Resistor

LTSpice Simulation: 10nF Ceramic Capacitor

Strategy 3: TVS Diodes

- Essentially act like a Zener diode.
  - *TVS diodes tend to have a faster response and a higher surge current rating.*
- **Reverse Working Maximum Voltage (VRWM):** The maximum reverse voltage that should be applied in normal operating conditions.
- **Breakdown Voltage (VBR):** The voltage where the diode just starts to conduct.
- **Clamping Voltage (VCLAMP):** The maximum voltage that the system will experience during a surge.
- **Dynamic resistance (RDYN):** The estimated resistance of the diod conducting.

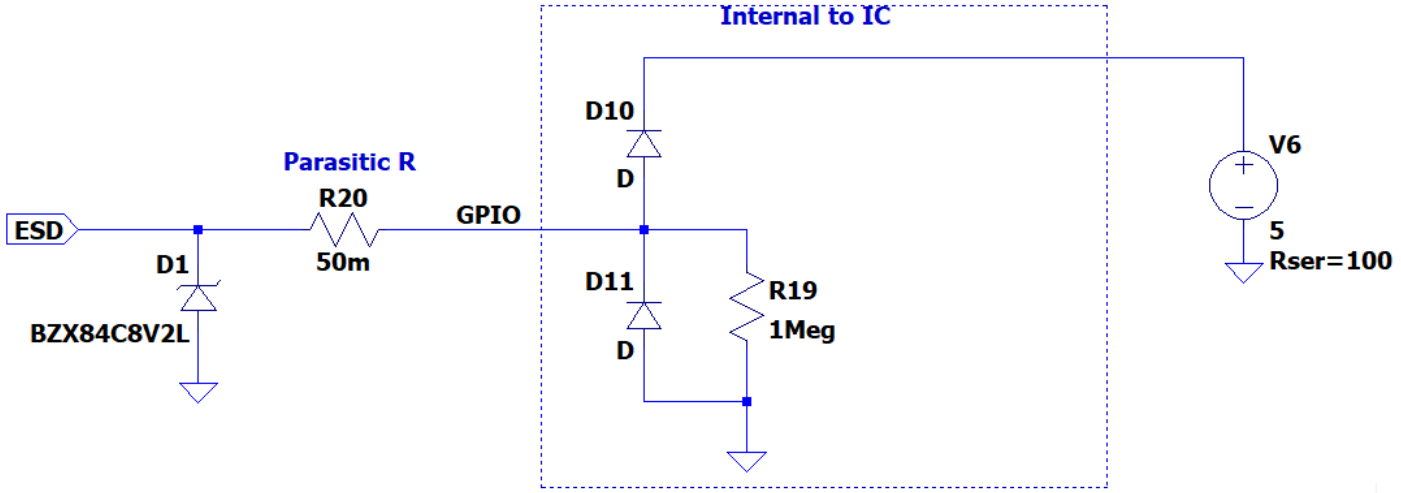


An ESD protection diode with low dynamic resistance helps reduce the amount of current that flows to the DUP.

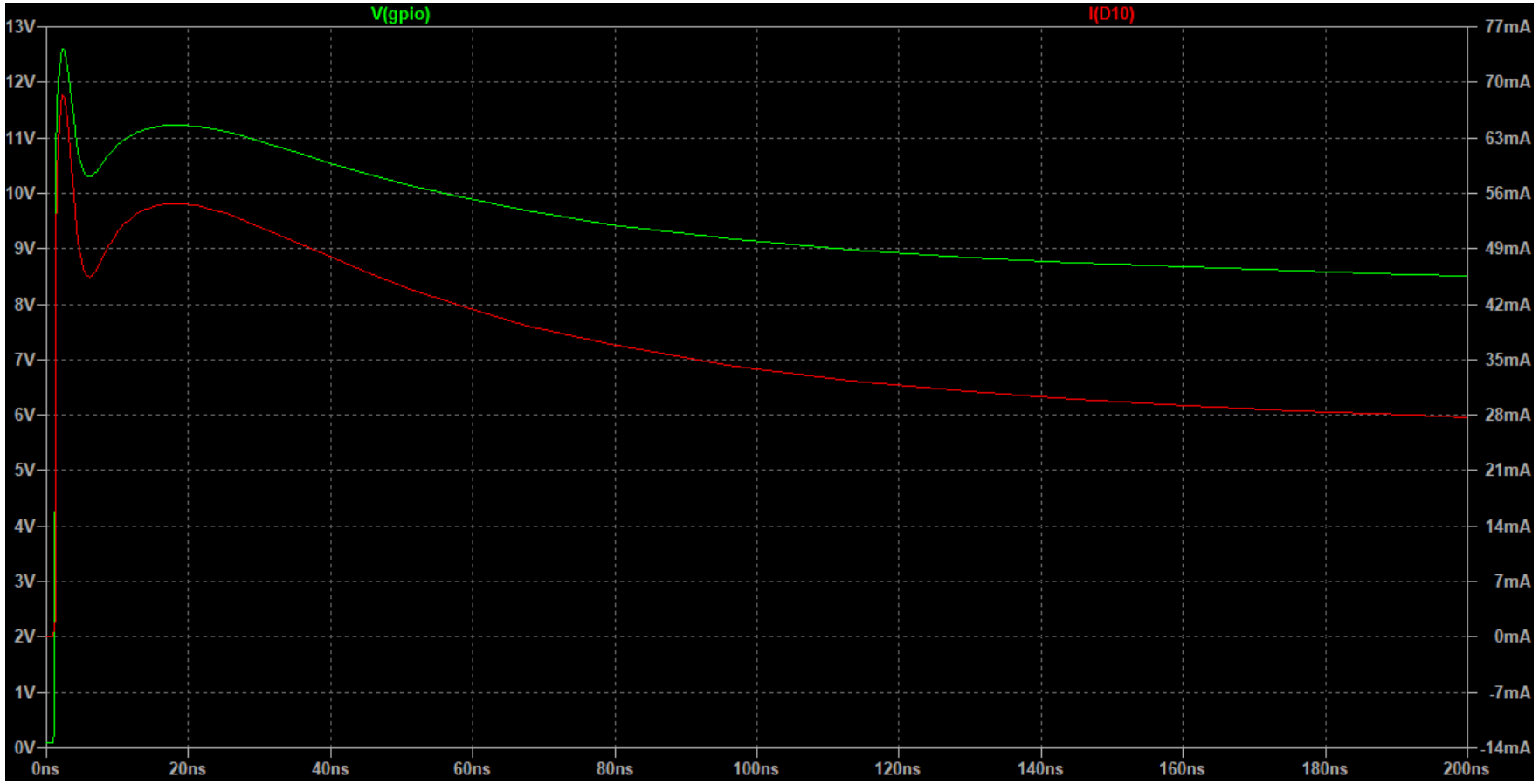
Basics of ESD Protection (TVS) Diodes - Toshiba

Strategy 3: TVS Diodes (Cont'd)

- Unidirectional TVS diodes protect from both positive and negative spikes.
- Bidirectional diodes only are needed for signals that go above and below 0V (RS485)
- TVS capacitance must be lower than the limit of whatever is being protected.



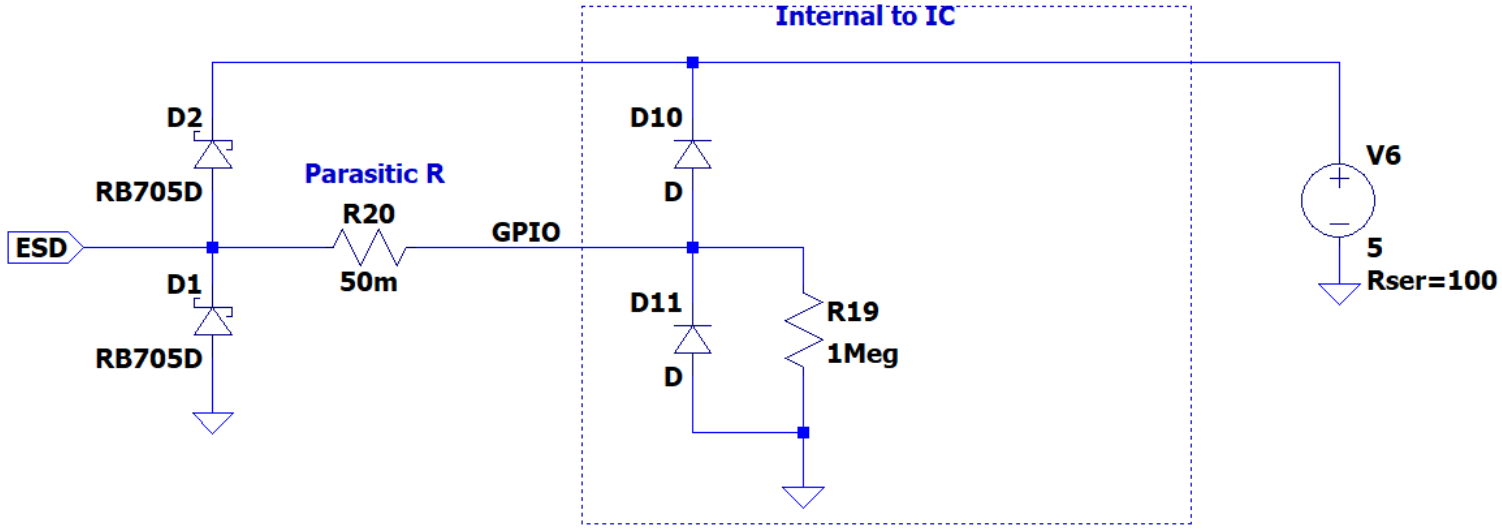
LTSpice Simulation: 8.2V Zener (TVS)



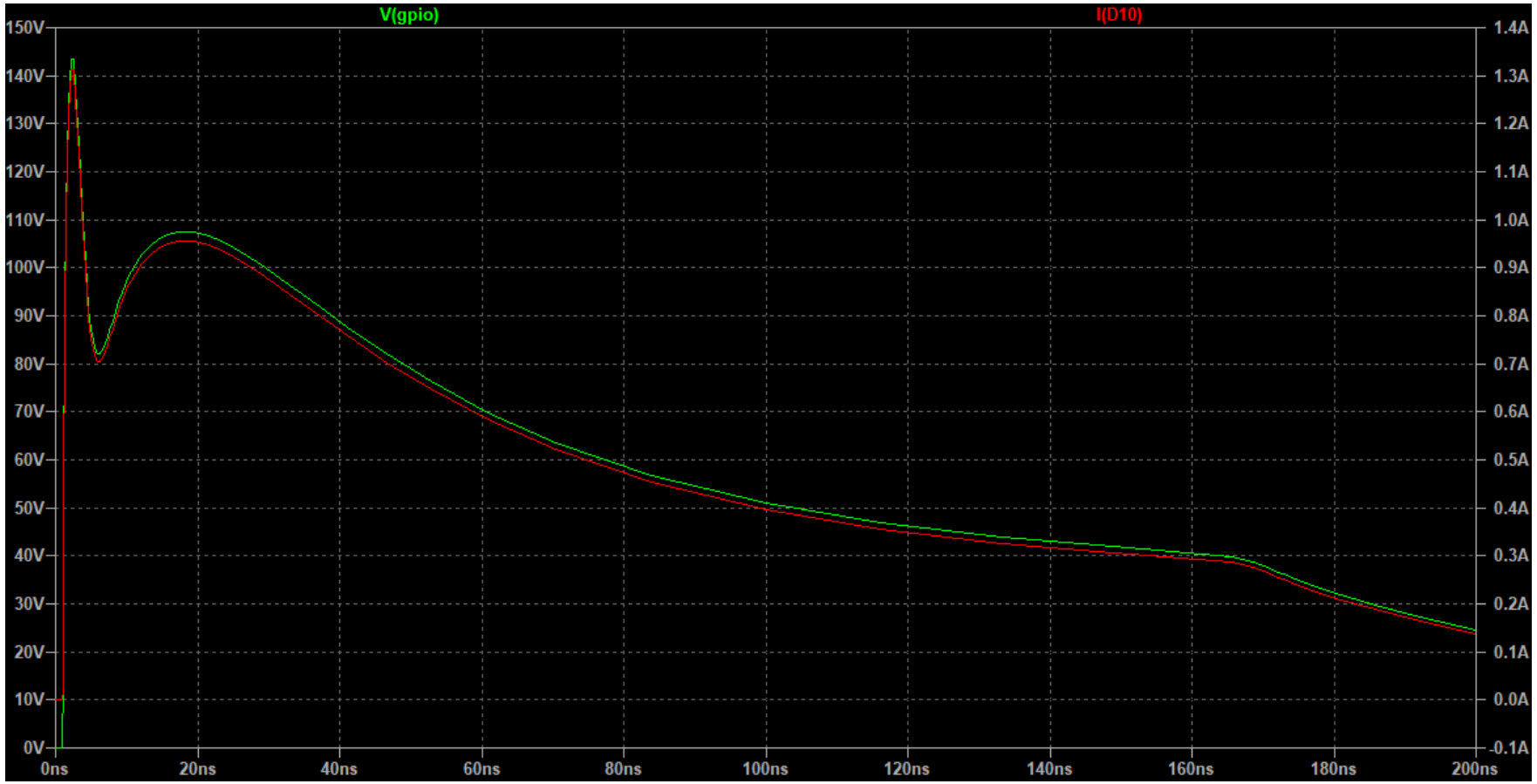
LTSpice Simulation: 10nF Ceramic Capacitor

Strategy 4: Dual Schottky Diodes

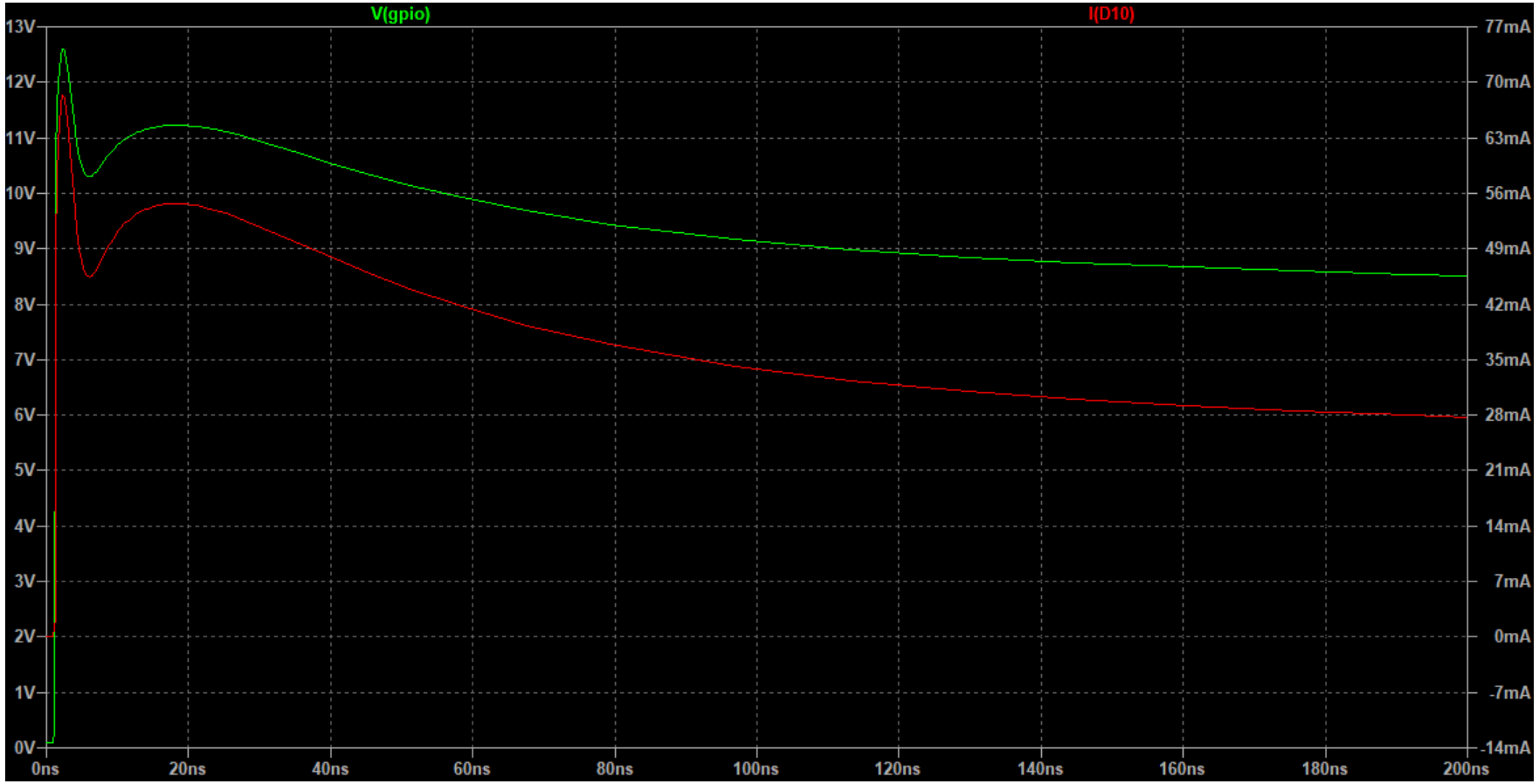
- The goal with dual Schottky's is to have them conduct before the internal diodes.
- This approach is highly dependent on the power rail impedance.
- This approach + series resistors can help limit current and overvoltage to input pins.



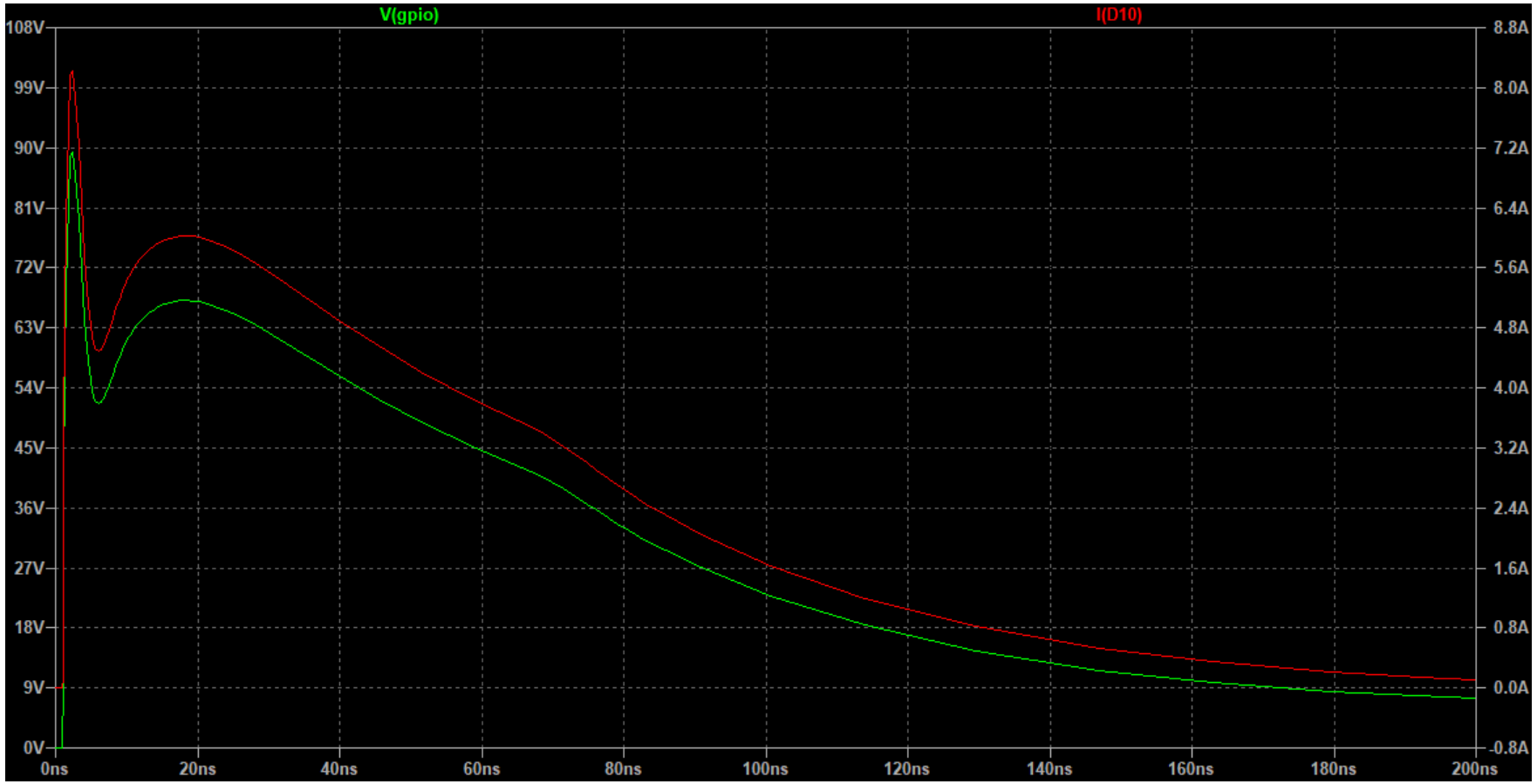
LTSpice Simulation: Dual Schottky Diodes (100R PSU Impedance)



LTSpice Simulation: 8.2V Zener (TVS)

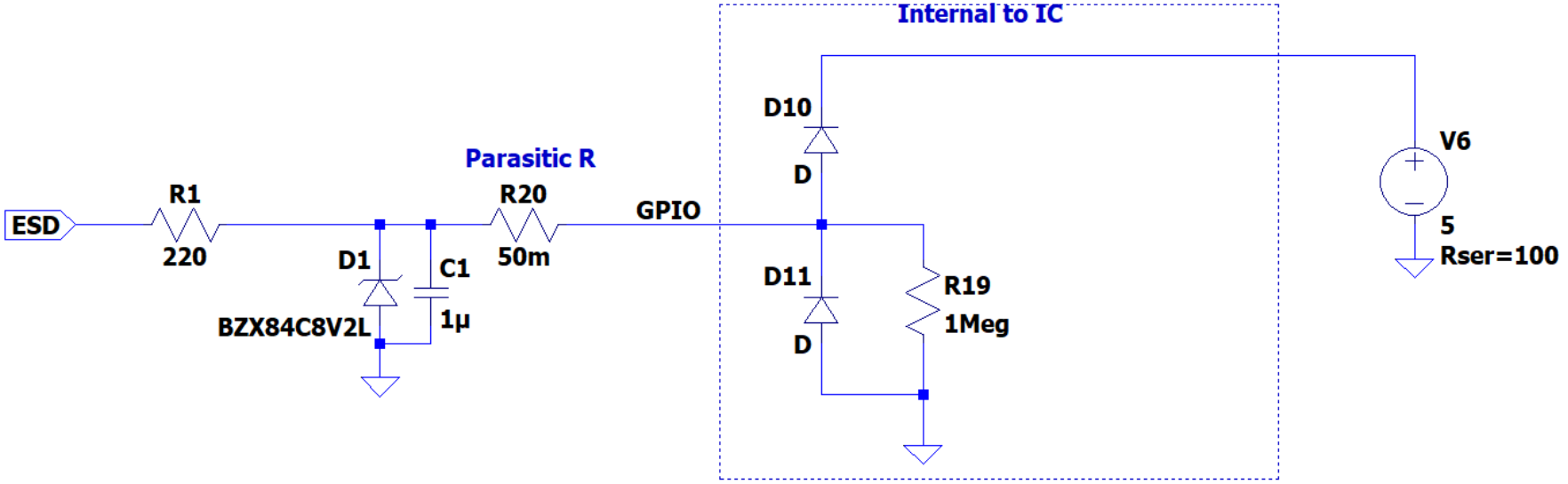


LTSpice Simulation: Dual Schottky Diodes (10R PSU Impedance)

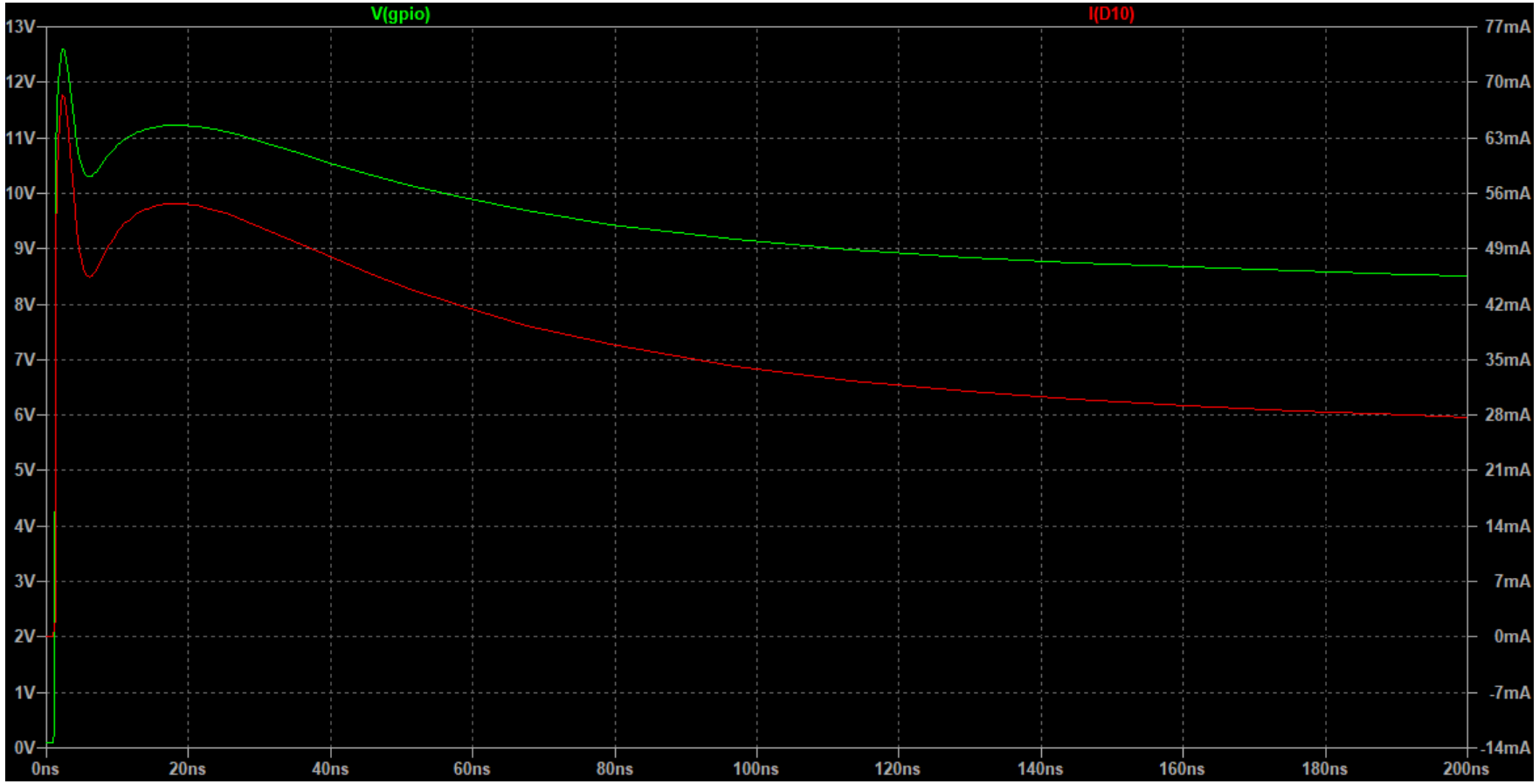


What Do I Normally use?

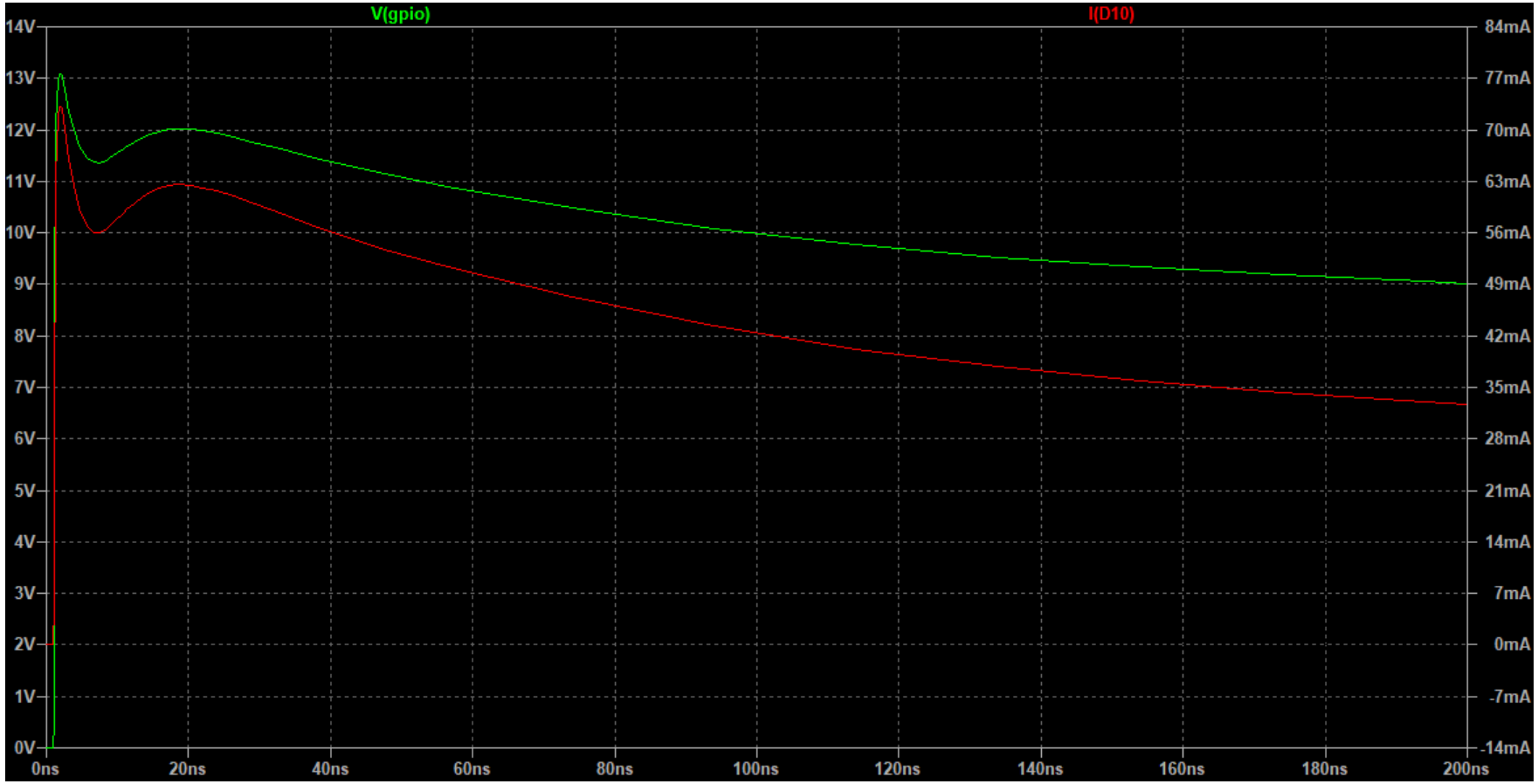
- **<u>High-Speed Interface (USB/Ethernet/HDMI/Etc.):</u>** A single TVS diode rated for that interface.
- **<u>Slow Interface, General Protection:</u>** Same as above, but will add a series resistor before the TVS.
- **<u>Slow Interface</u>** **Higher Protection:** Same as above, but will add a capacitor in pa



LTSpice Simulation: 8.2V Zener (TVS)



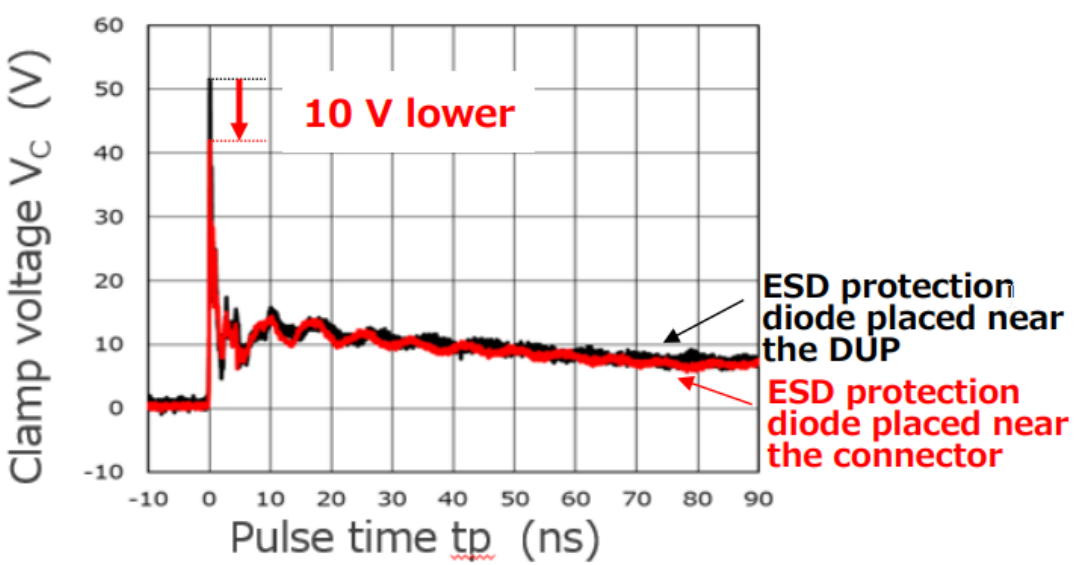
LTSpice Simulation: 8.2V Zener (TVS) + 220R



LTSpice Simulation: 8.2V Zener (TVS) + 220R + 1uF

PCB Layout considerations

- Protection needs to be as close to the connector/whatever as possible.
  - Low inductance traces.
- Don’t run protected traces near unprotected ones.
- Larger the ground plane, the better (e



Basics of ESD Protection (TVS) Diodes - Toshiba

Soft Failure Protection

- Primarily relates to firmware/software solutions.
- External watchdog monitor.
- CRC on all communication busses.
- Bit flip detection to force reset (RAM only).

Conclusion

- There is nearly an unlimited ways to protect a circuit.
- I showed 4 of the common ways that I do it
- It’s all about balancing cost/performance.
- When in doubt, use a TVS diode. If the signal is slow and you need additional protection, add in a series resistor or parallel capacitor.
- The software/firmware side can’t be ignored.